Amendments to the Specification

Please the replace paragraphs on page 20, lines 12-33 with the following amended paragraphs:

Bit line pair BL, /BL and write column select line CSLW are driven by power supply voltage VDDS for the array, whereas read column select line CSLR, write mask line ZWM, read data line pair /DLR, DLR, and write data line pair DLW, /DLW ~~/DLW, DLW~~ are driven by power supply voltage VDD for the peripheral circuitry.

Write column select gate 91 includes N channel MOS transistors 92 and 94 connected in series between node N28 and write data line DLW ~~/DLW~~ and N channel MOS transistors 93 and 95 connected in series between node N29 and write data line /DLW ~~DLW~~. The gates of N channel MOS transistors 92 and 93 are both connected to write mask line ZWM and the gates of N channel MOS transistors 94 and 95 are both connected to write column select line CSLW. When write mask line ZWM is at an 'H' level (VDD), if write column select line CSLW is turned to a select level, that is, an 'H' level (VDDS), by decoder band unit circuit 15, N channel MOS transistors 92~95 become conductive and nodes N28 and N29, that is, bit line BL, /BL and write data line DLW and /DLW ~~/DLW and DLW~~ are coupled, respectively, to perform the writing operation. When write mask line ZWM is at an 'L' level, N channel MOS transistors 92 and 93 of write column select gate 91 become nonconductive to electrically separate nodes N28 and N29, that is, bit lines BL, /BL from write data lines DLW and /DLW ~~/DLW and DLW~~, respectively, thereby prohibiting the data overwriting.